Amendments to the Specification:

Please replace paragraph [0036] with the following amended paragraph:

[0036] Figure 7 is a simplified diagram of one implementation of bidirectional switching circuits. The serial output from the node 1 P/S converter 68 is input into a tri-statable buffer 78. The buffer 78 has another input coupled to a voltage representing a high state. The output of the buffer 78 is the serial data which is sent via the line 85 to a Node 2 tri-statable buffer 84. A resistor 86 is coupled between the line 85 and ground. The Node 2 buffer 84 passes the serial data to a Node 2 S/P converter 72. Similarly, the serial output from the Node 2 P/S converter 74 is input into a tri-statable buffer 72. That buffer 72 also ~~having~~ has another input coupled to a high voltage. The serial output of that buffer 82 is sent via the line 85 to a Node 1 tri-statable buffer 80. The Node 1 buffer 80 passes the serial data to a Node 1 S/P converter 70.

Please replace paragraph [0047] with the following amended paragraph:

[0047] Figure 19 is a preferred implementation of the hybrid parallel/serial interface used between a GC controller 38 and ~~a GC 124~~ AGC 124. A data block, such as having 16 bits of GC control data (8 bits RX and 8 bits TX), is sent from the GC controller 38 to a data block demultiplexing device 40. The data block is demultiplexed into two nibbles, such as two eight bit nibbles. A start bit is added to each nibble, such as making 9 bits per nibble. The two nibbles are transferred over two lines using two P/S converters 42. The S/P converters 46 upon detecting the start bits convert the received nibbles to parallel format. The data block reconstruction device reconstructs the original 16 bits to control the gain of the GC 124. If a function is indicated by the start bits, such as in FIG. 11, the AGC 124 performs that function on the received block prior to adjusting the gain.